What Is Claimed Is:

1. A transposition circuit for generating data packets arranged as a transposed matrix and obtained from data packets in the form of an N × N matrix (where N is an integer of 2 or greater) by interchanging the rows and columns of the original matrix, wherein N input terminals and N output terminals are provided; and

N packets of data are outputted in parallel for each matrix column from said output terminals when N packets of data are inputted in parallel for each matrix row to said input terminals.

2. A transposition circuit as defined in claim 1, wherein said transposition circuit comprises a control unit and N × N registers arranged in N rows and N columns;

a first column of said registers and an N-th row of said registers are coupled with said input terminals;

a first row of said registers and an N-th column of said registers are coupled with said output terminals;

said control unit specifies a first transfer mode or a second transfer mode;

said first transfer mode involves performing a procedure in which data inputted to said input terminals is stored in the first column of said registers,

data stored in an *n*-th column (where *n* is an integer from 1 to (N - 1)) of said registers is transferred to an (*n* + 1)-th column of said registers, and

data stored in an N-th column of said registers is outputted to said output terminals; and

said second transfer mode involves performing a procedure in which data inputted to said input terminals is stored in the N-th row of said registers,

data stored in an *m*-th row (where *m* is an integer from 2 to N) of said registers is transferred to an (*m* - 1)-th row of said registers, and

data stored in the first row of said registers is outputted to said output terminals.

3. A transposition circuit as defined in claim 1, wherein said transposition circuit comprises N × N registers arranged in N rows and N columns, N × N first selectors whose output ports are individually connected to the input ports of these registers, (N - 1) second selectors whose output ports are individually connected to said output terminals, and a control unit;

said first and second selectors have first and second ports, and either the first or second ports are used as input ports in accordance with control signals from said control unit;

the first ports of said first selectors in an *i*-th row and a first column (where *i* is an integer between 1 and N), and the second ports of said first selectors in an N-th row and (N + 1 - *i*)-th column are connected to No. *i* input terminals;

the output ports of said registers in an *m*-th row and *n*-th column (where *m* is an integer between 2 and N, and *n* is an integer between 1 and (N - 1)) are connected to the second ports of said first selectors in an (*m* - 1)-th row and *n*-th column and to the first ports of said first selectors in the *m*-th row and (n + 1)-th column;

the output ports of said registers in the *m*-th row and N-th column are connected to the first ports of No. (*m* - 1) second selectors;

the output ports of said registers in a first row and *n*-th column are connected to the second ports of No. (N - *n*) second selectors;

the output ports of said registers in the first row and N-th column are connected to No. 1 output terminals; and

the output ports of No. *n* second selectors are connected to No. (n + 1) output terminals.

4. A transposition circuit as defined in claim 1, wherein said transposition circuit is provided with N memory units whose storage areas accommodate N data packets, N first selectors whose output ports are individually connected to the input ports of these memory units, N second selectors whose output ports are individually connected to said output terminals, and a control unit;

said first and second selectors have N ports, and any of these ports is used as an input port in accordance with selection signals from said control unit;

the ports of said first selectors are connected to the corresponding input terminals;

the ports of said second selectors are connected to the output ports of the corresponding memory units; and

said control unit specifies prescribed storage areas in said memory units and generates, together with said selection signals, address signals for reading data from said memory units and writing data to said memory units.